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CLAIMS

What is claimed is:

1. A system, comprising:

a voltage regulator and a clock generator to send a processor voltage or a processor clock, respectively;

a processor coupled to the voltage regulator to receive the processor voltage and the clock generator to receive the processor clock, respectively;

a control signal coupled to the processor, the voltage regulator, and the clock generator to prevent the processor from receiving the processor voltage and the processor clock until a fuse block programmed with a voltage configuration signal and a frequency configuration signal to specify the processor voltage and the processor clock frequency, respectively is determined to have a proper fuse block voltage.

2. The system of claim 1, wherein the voltage regulator is coupled to send the fuse block voltage to the processor and the control signal to the processor and the clock generator.

3. The system of claim 1, further comprising a second voltage regulator coupled to send the fuse block voltage to the processor and the control signal to the first voltage regulator, the processor, and the clock generator.

4. The system of claim 1, further comprising a second voltage regulator coupled to send the fuse block voltage to the processor, and wherein the first voltage regulator is coupled to sense the fuse block voltage and to send the control signal to the processor and the clock generator.

5. The system of claim 1, further comprising a transistor coupled to invert the control signal and send the inverted control signal to the clock generator.

6. A system, comprising:

a processor having programmable fuse block programmed with at least one configuration signal;

logic coupled to the processor to read the configuration signal and in response to generate a value specified by the configuration signal;

a control signal coupled to the processor and the logic to prevent the logic from reading the configuration signal until a predetermined event occurs.

7. The system of claim 6, wherein the configuration signal specifies a voltage for the logic to generate.

8. The system of claim 6, wherein the configuration signal specifies a frequency for the logic to generate.

9. The system of claim 6, wherein the predetermined event is when power to the programmable fuse block is valid and stable.

10. The system of claim 6, wherein the predetermined event is when the configuration signal is valid and stable.

11. A processor, comprising:

front-end logic to receive a control signal; and

configuration signal logic coupled to the front-end logic to inhibit booting up of the processor in response to the front-end logic receiving the control signal.

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12. The processor of claim 11, wherein the configuration signal logic is to inhibit booting up of the processor for a period of time.

13. The processor of claim 11, wherein the configuration signal logic is coupled to the front-end logic to inhibit booting up of the processor for a period of time after the configuration signal logic has power.

14. An apparatus, comprising:

a machine-readable medium having stored thereon instructions for causing a processor to:

apply a control signal to a processor from a voltage regulator to inhibit a platform normal boot process until at least one configuration signal can be read from a programmable fuse block in the processor.

15. The apparatus of claim 14, wherein the configuration signal specifies a voltage or a frequency to be received by the processor.

16. An apparatus, comprising:

a machine-readable medium having stored thereon instructions for causing a processor to:

receive a control signal to prevent a computer platform from booting until a voltage applied to a processor fuse block programmed with at least on configuration signal has reached a threshold level;

receive the control signal to permit the processor fuse block to be read;

configure the processor based on the configuration signals read from the fuse block; and

permit the computer platform to boot.

17. The apparatus of claim 16, wherein the instructions are further to cause the processor to receive a core voltage or a system bus clock, respectively, specified by the configuration signals.

18. The apparatus of claim 16, wherein the instructions are further to cause the processor to receive the control signal to permit the processor fuse block to be read when a fuse block voltage has reached a threshold value.

19. The apparatus of claim 16, wherein the instructions are further to cause the processor to receive the control signal to permit a clock generator or a voltage regulator to read the processor fuse block when a fuse block voltage has reached a threshold value.

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20. The apparatus of claim 19, wherein the instructions are further to cause the processor to receive a frequency signal or a voltage signal from the clock generator or voltage regulator after the clock generator or voltage regulator reads the processor fuse block.